Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) In a processing system having a <u>host</u> processor coupled to a system bus, a method of operating a <u>non-memory mapped</u> device <u>memory with respect to the host processor,</u> comprising:

    instructing the <u>host</u> processor to operate with the <u>non-memory mapped</u> device <u>memory</u>;

    putting information on the system bus<u>, wherein the information comprises both a</u>

        <u>command and an address embedded in a data stream</u>;

    retrieving the information with a memory map controller interface<u>, wherein responsive to</u>

        <u>the information, the memory map controller interface</u>

        <u>(i) selects the non-memory mapped device memory for a memory access if there are</u>

            <u>more than one,</u> [[;]]

        <u>(ii) downloads an appropriate access protocol</u> ~~accessing a~~ template of the <u>selected</u>

            <u>non-memory mapped</u> device <u>memory and performs a series of transactions to</u>

            <u>setup communication with the selected non-memory mapped device memory,</u>

            <u>wherein the appropriate access protocol template comprises a previously</u>

            <u>programmed template for each specific access type,</u> ~~with the memory map~~

            ~~controller interface responsive to the information;~~

        <u>(iii) inserts</u> ~~putting~~ device information ~~onto~~ <u>into an appropriate field of a message</u>

            structure on an external interface bus <u>for transfer to the non-memory mapped</u>

            <u>device memory</u> according to the information and the template; and

    operating <u>an actual data transfer with</u> the <u>non-memory mapped</u> device <u>memory</u> according

        to the device information, wherein the information comprises a mode of operation,

        chip select, access type, and an address.

2. (Currently Amended) The method of claim 1, wherein the <u>non-memory mapped</u> device <u>memory comprises a memory of</u> [[is]] an LCD controller, co-processor, peripheral device, graphic accelerator, imaging device or simply any peripheral with addressable registers or memory.

3. (Original) The method of claim 1, wherein the system bus contains an address bus.

4. (Original) The method of claim 1, wherein the information comprises a method of operation of the device.

5. (Original) The method of claim 4, wherein the method of operation is selected from a group consisting of read and write.

6.-25. (Canceled).